PATENT
8031-1028

**IN THE U.S. PATENT AND TRADEMARK OFFICE**

In re application of: Yoshihiro NONAKA
Conf.: 5218

Appl. No.: 10/648,256
Group: 2811

Filed: August 27, 2003
Examiner: Ori Nadav

Title: SEMICONDUCTOR INTEGRATED CIRCUIT, METHOD OF MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT, CHARGE PUMP CIRCUIT, LAYOUT DESIGNING APPARATUS, AND LAYOUT DESIGNING PROGRAM

**RESPONSE**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

March 11, 2005

Sir:

This replies to the Official Action mailed January 11, 2005.

**Remarks** begin on page 2 of this paper.